BRisbane Silicon

DPTx 1.4

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NOTE: specifications are based on AMD/Xilinx 28nm fabric

Specifications

Footprint

1000	Slice LUTs (min)
3500	Slice LUTs (max)
2300	Slice Registers (min)
4200	Slice Registers (max)
0	BRAM

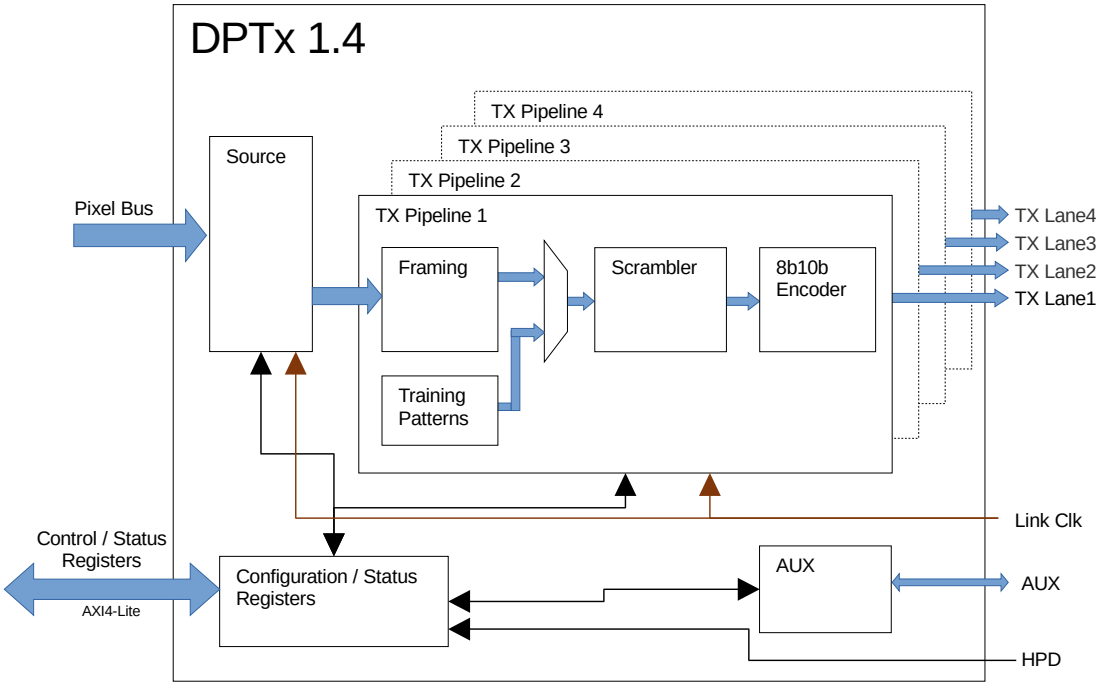
Performance

400 MHz	FMax

Features

- Ultra-small footprint (min 1k LUT).
- Static, compile-time framing configuration.
- Simulation testbench, including software verification harness.
- Hardware proven.
- Example project, which demonstrates IP core bring-up and 4k60 video test pattern.

Block Diagram



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Example Project

Target Numato Lab Mimas A7

Description The Microblaze hosts the Link Policy Maker firmware, which, upon HPD, initializes the DP1.2 TX PHY and DPTx1.4 core. The link training procedure is then performed, and once it successfully completes, the TFG is enabled to produce a configurable test pattern at a video framing of 4k60.

Block Diagram