BRisbane Silicon

DP1.2 TX PHY

DP1.2 TX PHY

NOTE: this IP is Xilinx platform specific
NOTE: specifications are based on Xilinx 28nm fabric

Specifications

Footprint

250	Slice LUTs
1200	Slice Registers
0	BRAM
4	GTPE2_CHANNEL
1	GTPE2_COMMON
1	MMCME2_ADV

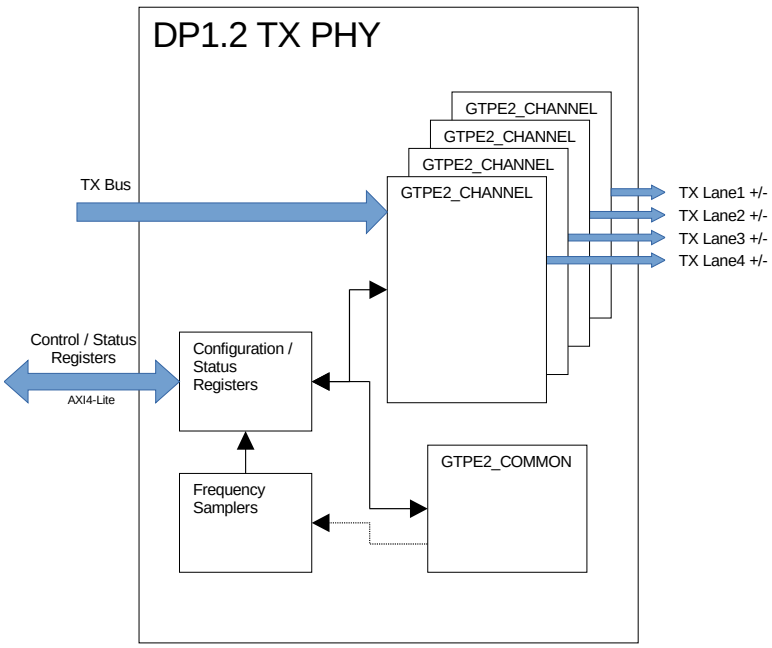
Performance

270 MHz	FMax

Features

- Supported link rates of 1.62, 2.7 and 5.4 Gbps.
- Hardware proven.
- Simulation testbench.
- Example project, including firmware which performs link initialization with the PHY.

Block Diagram



DP1.2 Tx PHY

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NOTE: specifications are based on Xilinx 28nm fabric

Example Project

Target Numato Lab Mimas A7

Description The Microblaze hosts the Link Policy Maker firmware, which, upon HPD, initializes the DP1.2 TX PHY with the configured link rate. The link training procedure is then performed to demonstrate correct functioning of the DP1.2 TX PHY.

Block Diagram